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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03K 17/56, 17/687, 17/74, H01L 29/788 — A1

(11) International Publication Number: **WO 98/16010**

(43) International Publication Date: 16 April 1998 (16.04.98)

(21) International Application Number: PCT/US96/16317

(22) International Filing Date: 10 October 1996 (10.10.96)

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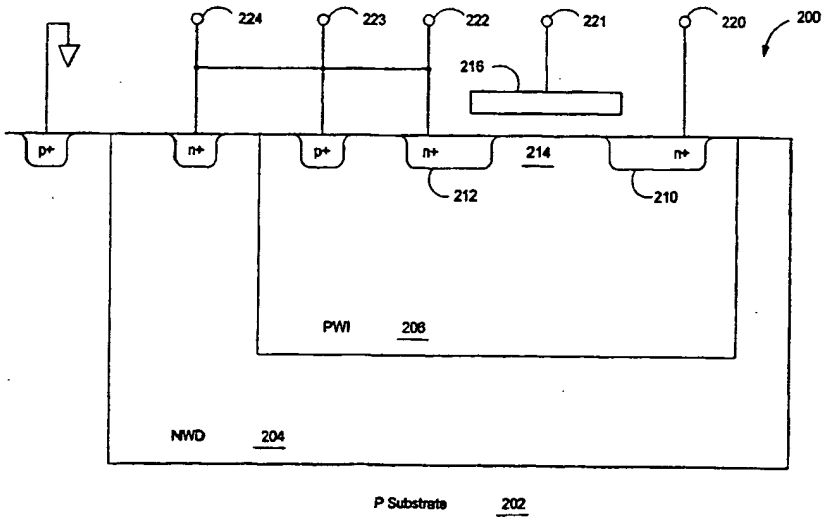
(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

With international search report.

(54) Title: TRIPLE WELL CHARGE PUMP



(57) Abstract

An improved charge pump design. This charge pump comprises at least one pumping transistor having a triple well arrangement (206, 204, 206). This triple well pump transistor has a source and a drain (210, 212) of a first conductive type formed on a first well (206) having an opposite conductive type. A second well (204) having the first conductive type is formed outside of the first well (206). The source region, first well and second well are set to substantially the same potential. One aspect of this configuration is that the first well forms a semiconductor diode with the drain region (212). Another aspect of this arrangement is that the body effect of the transistor is reduced. The reduction in body effect reduces the threshold voltage of the transistor. It is found that the above mentioned diode and threshold voltage of the tansistor, singly and in combination, allow the charge pump to operate more efficiently.

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TRIPLE WELL CHARGE PUMP

FIELD OF THE INVENTION

The present invention relates to charge pump circuits, and more particularly to using trip well transistors in the design of charge pump circuits.

BACKGROUND OF THE INVENTION

A charge pump is a circuit that can generate an output voltage that is higher than the voltage supplied to the charge pump. One of the applications of charge pumps is to develop voltage for erasing and programming some kinds of nonvolatile semiconductor memory devices, such as electrical erasable programmable read only memory (EEPROM) and flash memory. One way to operate these memory devices is to program through hot electron injection and erase through Fowler-Nordheim tunneling. The programming and erasing of such a memory cell require current to pass through the dielectric surrounding a floating gate electrode. As a result, a high voltage is generally needed. Some prior art nonvolatile semiconductor memory devices require the application of an external high voltage (e.g, 12 volts) in addition to a regular 5 volts supply voltage. This arrangement is undesirable because it is complicated and wastes real estate on circuit boards. Recently, many nonvolatile semiconductor memory device manufacturers place charge pumps on chip so as to develop the required high voltage for erasing and programming. Many customers welcome this development, and the sale of nonvolatile semiconductor devices increases.

As the number of memory cells in a nonvolatile semiconductor memory device increases, the current required to erase and program these cells also increases. As a result, there is a need for the charge pump to be efficient, e.g., generating more current and at a faster rate.

SUMMARY OF THE INVENTION

The present invention relates to using triple well transistors to increase the efficient of a charge pump. The inventive charge pump comprises a plurality of pumping transistors arranged to increase the voltage level from a first pumping transistor to a last pumping transistor in response to clock pulses applied to these pumping transistors. At least one of the plurality of pumping transistors has a source and a drain region of a first conductive type formed on a first well having an opposite conductive type.

A second well having the first conductive type can be formed outside of the first well. The second well is fabricated on a substrate. This transistor design is commonly referred to as a "triple well" transistor. The source region, first well and the second well is preferably set to substantially the same potential. In one embodiment of the present invention, the second well can be set to the highest positive potential of the charge pump.

One aspect of this configuration is that the first well forms a semiconductor diode with the drain region. This diode allows more current to flow through the pumping transistor, when compared with a pumping transistor of conventional construction. Another aspect of this arrangement is that it reduces the body effect of the triple well transistor. As a result, the threshold voltage of the transistor is reduced. The reduction in threshold voltage allows the transistor to be turned on faster.

It is found that the above mentioned diode and threshold voltage reduction effects, singly and in combination, allow the charge pump to operate more efficiently. Example of the improved efficiency include increasing the output current, lowering the power supply voltage level, and increasing the operating frequency.

The triple well pumping transistor of the present invention can be used in positive voltage and negative voltage charge pumps.

These and other features of the present invention will become apparent from the following detailed description of the invention read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a four-stage charge pump of the present invention.

Fig. 2 shows timing diagram of clock pulses that can be used with the charge pump of Fig. 1.

Fig. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor of the present invention.

Fig. 4 is the top view of four triple well transistors of the present invention that can be used in the charge pump of Fig. 1.

Fig. 5 shows voltage profiles at various points of the charge pump of Fig. 1.

Fig. 6 is a schematic diagram of a negative voltage charge pump of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention related to a novel charge pump system. The following description is presented to enable any person skilled in the art to make and use the invention. Descriptions of specific applications are provided only as examples.

Various modifications to the preferred embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

Fig. 1 is a schematic diagram of a four-stage charge pump 100 of the present invention. Charge pump 100 comprises nine triple well NMOS transistors 102-110 and twelve normal NMOS transistors 112-119 and 132-135. These normal NMOS transistors are preferably native n-channel devices that have a low threshold voltage. Normal NMOS transistors 132-135 function as pull up transistors. Normal NMOS transistors 112-119 function as capacitors, and are coupled to clock pulses 122-129. The clock pulses are coupled to the corresponding triple well NMOS transistors via the capacitive action of transistors 112-119. Although there are eight clock pulses, they are arranged in pairs: (122,124), (123,125), (126,128), and (127,129). Each clock pulse in a pair has the same pulse timing while different pairs have different pulse timings. The clock pulses are shown in Fig. 2 where timings 192-195 correspond to pairs (127,129), (122,125), (126, 128) and (123, 125), respectively. These pulses alternatively boost up the gates of these capacitors. This results in an increase in voltage level from stage to stage. The way voltage is being pumped up is similar to a conventional charge pump. In one embodiment of the present invention, the output voltage at the drain terminal of triple well NMOS 110 is approximately 10.5 volts while the voltage supplied to charge pump 100 is only 3 volts. As explained in detail below, the use of these triple well transistors (instead of normal NMOS transistors) enhances the performance and efficiency of charge pump 100 compared to prior art four-stage charge pumps.

It should be noted that a charge pump preferably includes other associated circuits, e.g., precharge and voltage regulation circuits. These circuits are well known by persons of ordinary skill in the art, and will not be described here.

Fig. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor 200 that can be used for transistors 102-110 of Fig. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed on top of substrate 202, and a P well 206 is formed on top of N well 204. An N+ type drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220-224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

In one embodiment of the present invention, the potential of source region 212, P well 206 and N well 204 are set to the same value. One way to meet this condition is to electrically connecting terminals 222, 223 and 224. The potential of substrate 202 is normally set to ground. This arrangement creates a PN diode between P well 206 and drain region 210. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an "extra diode." As explained in more detail below, this extra diode has the following advantageous effects:

(1) The size of the pass gate of the triple well NMOS transistors 102-109 can be reduced because some of the current for charging the next stage NMOS capacitors (i.e., transistors 112-119) can be conducted by the extra diode.

(2) Because the size of the NMOS transistors 102-109 can be reduced, their parasitic capacitor is reduced. As a result, less power is consumed and the pump output current can be increased.

(3) This low resistance extra diode path increases the forward conduction current. It can increase the pumping frequency because charges can be built up faster.

(4) The extra diode conduction path reduces the peak voltage swing at the output transistor 110 from $V_{DD}+V_{out}$ to $0.7+V_{out}$ volts, where V_{DD} is the power supply voltage and V_{out} is the output voltage at an output terminal 138 of charge pump 100. As a result, the internal voltage stress of the charge pump is reduced.

As a result of the above mentioned advantages, the performance of charge pump 100 improves tremendously by the presence of this diode. This benefit is achieved without requiring any silicon real estate.

Another advantage of this arrangement is that the body effect is suppressed. Body effect arises when the source and substrate is reverse biased. It is well known that the threshold voltage of a NMOS transistor is given by:

$$V_T = V_{T0} + \gamma \sqrt{[(V_{BS} + V_{BI})^2 - (V_{BI})^2]},$$

where V_{T0} is the threshold voltage when there is no substrate bias, V_{BS} is the potential between the source and the body, and V_{BI} is the voltage difference of a P-N junction if no external voltage is applied (i.e., zero bias). The typical values for V_{T0}, V_{BI} and γ are 0.7 volt, 0.7 volt, and 0.4, respectively.

It can be seen from the above equation that applying a voltage across a reverse-biased source-substrate junction tends to increase the threshold voltage of a transistor. In the triple well transistor of the present invention, V_{BS} is limited within the P-N junction cut-in voltage of 0.7 volt. This is because when pumping is activated, charge flows from N+ diffusion region 212 to N+ diffusion region 210 through channel 214 and the extra diode created by well 206 and region 210. Thus, the lower potential N+ diffusion region 210, which is the source, suffers minimized substrate bias around 0.7 volt which is much less as compared to more than 10 volts of substrate bias in prior art regulator NMOS charge pumps. In a charge pump circuit, it is important to generate high forward conduction current so that charges can be build up quickly. A low threshold voltage allows the NMOS channels to be turned on faster, and thus can increase the pumping frequency. Because the threshold voltage of the triple well NMOS transistor of the present invention is very low, the pumping frequency of the present inventive charge pump can be much higher than prior art charge pumps. In an embodiment of the present invention, the charge pump can operate efficiently at 22 MHz while prior art charge pump typically operates at 10 MHz.

Fig. 4 shows a top view 250 of four triple well transistors used in the present invention. It shows two transistor 252 and 254 formed inside a P well 258 and an N well 256. Transistor 252 further comprises a gate 260, a source region 262 and a drain region 264. Transistor 252 could correspond to transistor 102 of Fig. 1. Transistor 254 further comprises a gate 270, a source region 272 and a drain region 274. Transistor 254 could correspond to transistor 106 of Fig. 1.

Fig. 4 also shows two transistor 282 and 284 formed inside a P well 288 and an N well 286. Transistor 282 further comprises a gate 290, a source region 292 and a drain region 294. Transistor 282 could correspond to transistor 103 of Fig. 1. Transistor 284 further comprises a gate 280, a source region 282 and a drain region 284. Transistor 284 could correspond to transistor 107 of Fig. 1.

Referring to both Figs. 1 and 4, the source terminal 141 of transistor 102 and source terminal 142 of transistor 106 are connected to V_{DD}. Thus, source regions 262 and 272 of transistors 252 and 254, respectively, have the same potential (i.e., V_{DD}). As explained above, P well 258 and N well 256 should have the same potential as source regions 262 and 272. Thus these two wells also have the same potential (V_{DD}).

Fig. 1 shows that the gate terminal 144 of transistor 102 is connected to the drain terminal 145 of transistor 106, the source terminal 146 of transistor 103 and the source terminal 147 of transistor 107. As explained above, P well 288 and N well 286 should have the same potential as source regions 292 and 302 (which are coupled to source terminals 146 and 147). Thus in Fig. 4, gate 260, drain region 274, source regions 292 and 302, N well 286 and P well 288 all have the same potential.

Fig. 1 shows that the drain terminal 150 of transistor 102 is connected to the gate 151 of transistor 106. Thus, in Fig. 4, drain region 264 has the same potential as gate 270.

Fig. 1 shows that the gate terminal 153 of transistor 103 is connected to the drain terminal 154 of transistor 107 (in addition to the source terminals 155 and 156 of transistors 104 and 108). Thus in Fig. 4, gate 290 has the same potential as drain region 304. Fig. 1 also shows that the drain terminal 158 of transistor 103 is

connected to the gate 159 of transistor 107. Thus, in Fig. 4, drain region 294 has the same potential as gate 300.

In Fig. 4, only four of the nine triple well NMOS transistors comprising a charge pump are shown. The structure of transistors 104-105 and 108-109 is similar to that shown in Fig. 4. The structure of transistor 110 is similar to that of transistor 254 of Fig. 4.

In one embodiment of the present invention, the channel length of all the triple well transistors are 1.2 μm. The channel width of transistors 252 and 282 (corresponding to transistors 102 and 103 of Fig. 1) is 6 μm while the channel width of transistors 254 and 284 (corresponding to transistors 106 and 107 of Fig. 1) are 18 μm. Transistors 104 and 105 have the same structure as transistors 102 and 103, respectively. Thus, these two transistors also have a channel length of 1.2 μm and a channel width of 6 μm. Transistors 108 and 109 have the same structure as transistors 106 and 107, respectively. Thus, these two transistors also have a channel length of 1.2 μm and a channel width of 18 μm. For the output transistor 110 of Fig. 1, the channel width is 15 μm.

The dimension of normal transistors 112-119 and 132-135 of the same embodiment is shown in Table 1.

TABLE 1

Transistor	Channel Length (μm)	Channel Width (μm)
112	10	18
113	10	18
114	20	18
115	20	24
116	120	60
117	120	60
118	120	60
119	120	60
132	1.2	4
133	1.2	4
134	1.2	4
135	1.2	4

In order to determine the improvement of the triple well transistors over normal transistors in a charge pump, four tables showing the pump load lines are presented below. In each table, the two right hand columns correspond to the load line of a charge pump constructed using the preferred triple well transistor of the present invention. The two columns to the left of these two right hand columns correspond to the load line of the same charge pump constructed using normal transistors. It is observed that the inventive charge pump has a higher current at almost all voltage levels.

TABLE 2: pump load line, V_{DD}=2v, temp=25 C

I_{out} measure by root-mean-square, unit in mA

V_{out}/I_{out}	Prior Art-4-Phase 7.3MHz	Prior Art-4-Phase 22 MHz	Preferred-4-Phase 7.3MHz	Preferred-4-Phase 22 MHz
10v	0.0	0.0	0.0	0.0
9v	0.0	0.0	0.01	0.02
8v	0.01	0.01	0.04	0.1
7v	0.04	0.05	0.09	0.24
6v	0.08	0.12	0.19	0.48
5v	0.14	0.19	0.27	0.75

TABLE 3: pump load line, V_{DD}=2v, temp=25 C

I_{out} measure by average, unit in mA

V_{out}/I_{out}	Prior Art-4-Phase 7.3MHz	Prior Art-4-Phase 22 MHz	Preferred-4-Phase 7.3MHz	Preferred-4-Phase 22 MHz
10v	0.0	0.0	0.0	0.0
9v	0.0	0.0	0.01	0.02
8v	0.01	0.01	0.03	0.9
7v	0.04	0.05	0.06	0.17
6v	0.06	0.11	0.08	0.25
5v	0.09	0.166	0.10	0.31

TABLE 4: pump load line, V_{DD}=3v, temp=25 C

I_{out} measure by Root-mean-square, unit in mA

V_{out}/I_{out}	Prior Art-4-Phase 7.3MHz	Prior Art-4-Phase 22 MHz	Preferred-4-Phase 7.3MHz	Preferred-4-Phase 22 MHz
10v	0.11	0.266	0.29	0.75
9v	0.176	0.396	0.05	1.39
8v	0.256	0.548	0.75	1.6
7v	0.341	0.712	0.92	1.75
6v	0.419	0.799	1.25	1.8
5v	0.47	0.952	1.35	1.98

TABLE 5: pump load line, V_{DD}=3v, temp=25 C

I_{out} measure by average, unit in mA

V_{out}/I_{out}	Prior Art-4-Phase 7.3MHz	Prior Art-4-Phase 22 MHz	Preferred-4-Phase 7.3MHz	Preferred-4-Phase 22 MHz
10v	0.078	0.217	0.107	0.302
9v	0.108	0.300	0.128	0.423
8v	0.137	0.386	0.157	0.460
7v	0.167	0.468	0.178	0.496
6v	0.190	0.520	0.205	0.504
5v	0.203	0.597	0.222	0.532

The result shown in Tables 2-5 shows the following:

(1) The charge pump of the present invention functions efficiently at low V_{DD} voltage. For example, the performance improvement of the inventive charge pump over prior art charge pumps at V_{DD} = 2 volts is greater than that at V_{DD} = 3 volts. It is found that the inventive charge pump can operate effectively down to 1.5 volt.

(2) The charge pump of the present invention can operate efficiently at 22 MHz. For example, Table 2 shows that the output current for the inventive charge pump at 22 MHz is about 2.5 times that at 7.3 MHz (V_{out} = 7 v). On the other hand, there is little difference in the output current of a prior art charge pump at 22 MHz and 7.3 MHz.

The operation of charge pump 100 is now explained. Fig. 5A-5C show voltage profiles at nodes 161-168 and 138 of Fig. 1. Fig. 5A shows four clock pulses which are the same as pulses 124, 125, 128 and 129 of Fig. 2. These clock pulses are shown here again so as to provide a reference to understand the voltage profiles. Fig. 5B shows the voltage profiles 361-365 at nodes 165-168 and 138, respectively. Fig. 5C shows the voltage profiles 366-369 at nodes 161-164, respectively. It can be seen at regions 371-373 of Fig. 5B that charges are being pumped to subsequent stages when the triple well transistors 107-109 are turned on. As a result, the voltages of the two adjoining stages are equal at these regions. This pumping effect is enhanced by the extra diode and reduced threshold voltage of the corresponding triple well transistor of the present invention. The improved effect of other triple well transistors can be easily analyzed by person skilled in the art, and will be not explained in detail here.

The present invention can be applied to a negative charge pump having a negative output voltage. Fig. 6 is a schematic diagram of a negative charge pump

500 in accordance with the present invention. Charge pump 500 comprises eleven triple well NMOS transistors 502-512 and ten P-channel transistors 522-531. These P-channel transistors function as capacitors, and are coupled to clock pulses 534-543. The clock pulses are coupled to the corresponding triple well NMOS transistors via the capacitive action of transistors 522-531. Four P-channel transistors 550-553 can be optionally connected to the source terminals of triple well transistors 508-511 for initial pull-down purpose. In one embodiment of the present invention, the output voltage at the drain terminal of triple well NMOS 512 is approximately -8 volts when the voltage supplied to charge pump 500 is approximately 3 volts. The use of a triple well structure in transistors 502-512 suppresses the body effect and introduces an extra diode in the same way as discussed above in connection with charge pump 100. Thus, all the beneficial effects described above is also present in charge pump 500.

While several embodiments have been disclosed, it will be readily apparent to those skilled in the art that numerous other modifications and variations not mentioned above can still be made without departing from the spirit and scope of the invention claimed below. For example, the above disclosed triple well structure is not limited to be used in the charge pump design of Figs. 1 and 6, but instead can be used in practically all charge pump circuits.

CLAIMS:

1. A charge pump comprising:

a plurality of transistors arranged to increase voltage level from a first transistor to a last transistor in response to clock pulses, said last transistor having a voltage level substantially higher than a power supply voltage coupled to said plurality of transistors; and

at least one of said plurality of transistors having a source and a drain region of a first conductive type formed on a first well having an opposite conductive type, thereby forming a semiconductor junction between said first well and said source and said drain regions, said one transistor being formed on top of a substrate.

2. The charge pump of claim 1 wherein said source region and said first well have substantially the same potential.

3. The one transistor of claim 1 further comprising a second well having said first conductive type, said second well formed outside of said first well and on top of said substrate.

4. The one transistor of claim 1 further comprising a second well having said first conductive type, said second well formed outside of said first well and on top of said substrate said source region, said first well and second well have substantially the same potential, thereby substantially reducing body effect of said one transistor.

5. The charge pump of claim 4 wherein said power supply voltage is in an approximate range between 5 and 1.5 volts.

6. The charge pump of claim 4 wherein said power supply voltage being substantially equal to 3 volts.

7. The charge pump of claim 4 wherein said power supply voltage being substantially equal to 2 volts.

8. The charge pump of claim 4 wherein at least one of said clock pulses operates at a frequency above 10 MHz.

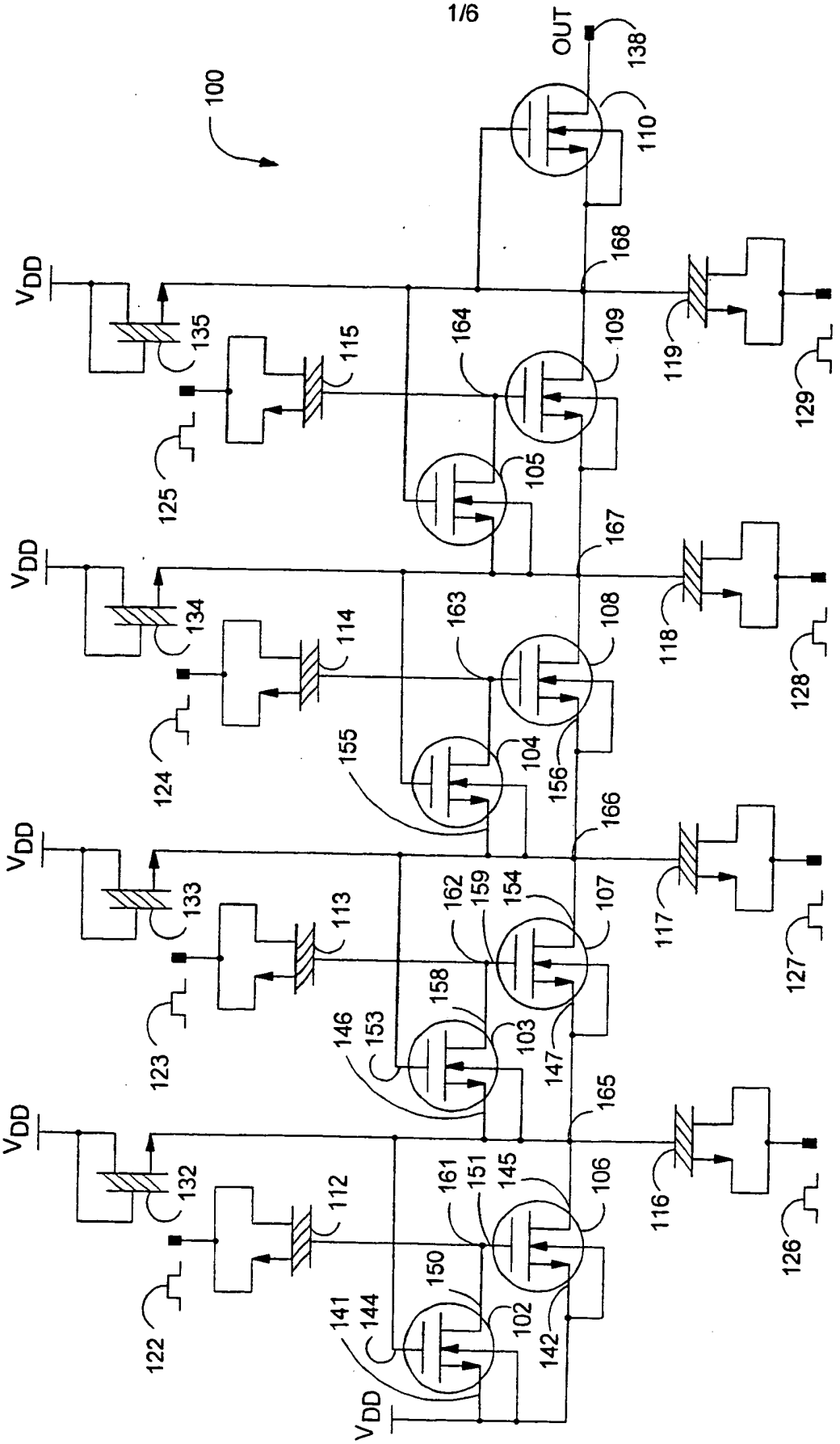
9. The charge pump of claim 4 wherein at least one of said clock pulses operates at a frequency approximately equal to 22 MHz.

10. The charge pump of claim 1 wherein said voltage level at said last transistor is positive.

11. The charge pump of claim 1 wherein said voltage level at said last transistor is negative.

12. The charge pump of claim 1 further comprising means for coupling said clock pulses to said transistors.

13. The charge pump of claim 12 wherein said means for coupling comprising a MOS transistor.


100
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138
110
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V_{DD}
135
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125
164
109
105
119
129
167
134
114
124
163
108
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118
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155
156
166
133
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158
146
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FIG.1

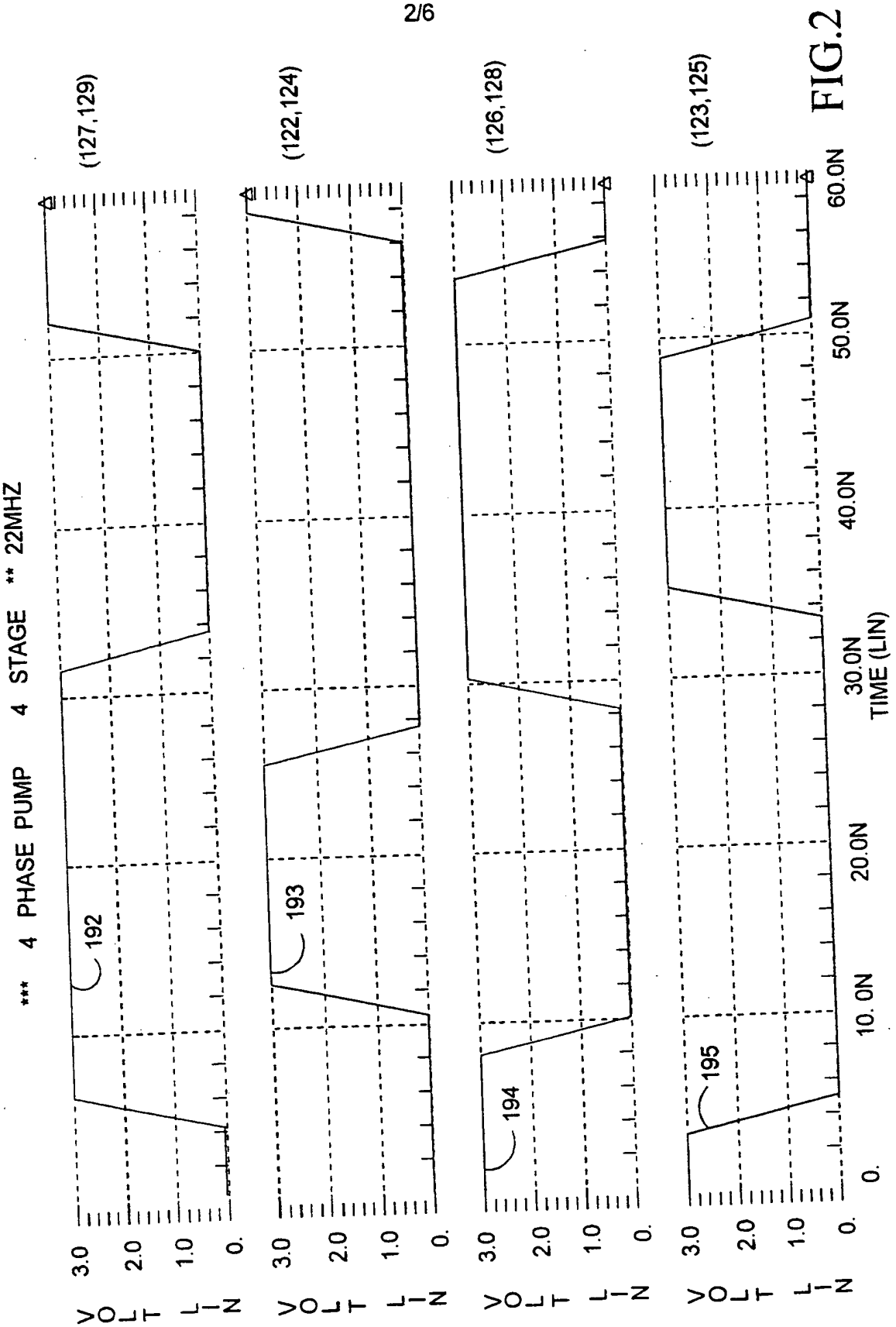

*** 4 PHASE PUMP 4 STAGE ** 22MHZ
(127,129)
(122,124)
(126,128)
(123,125)
192
193
194
195
VOLT L-N
3.0
2.0
1.0
0.
10.0N
20.0N
30.0N
40.0N
50.0N
60.0N
TIME (LIN)

FIG.2

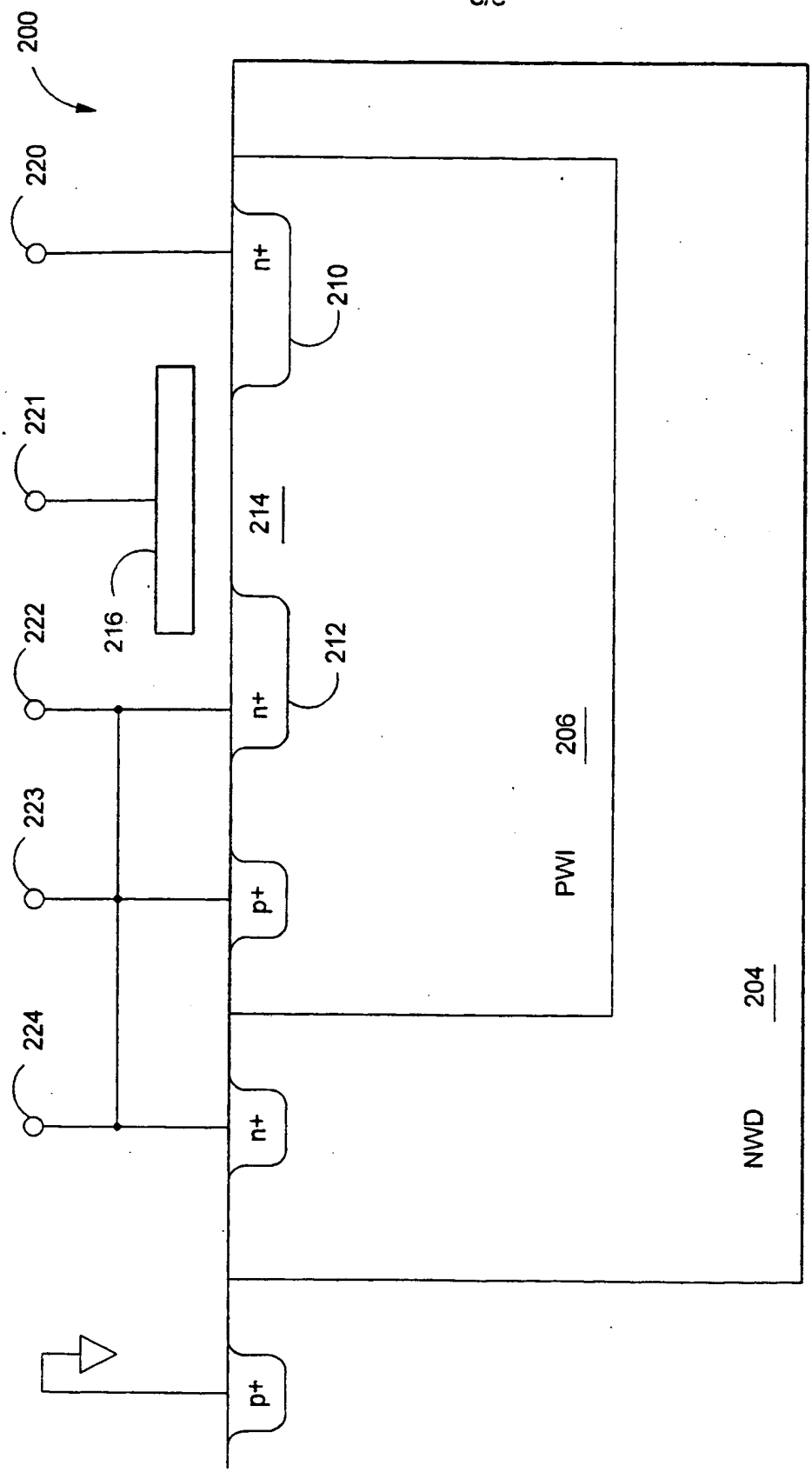


FIG.3

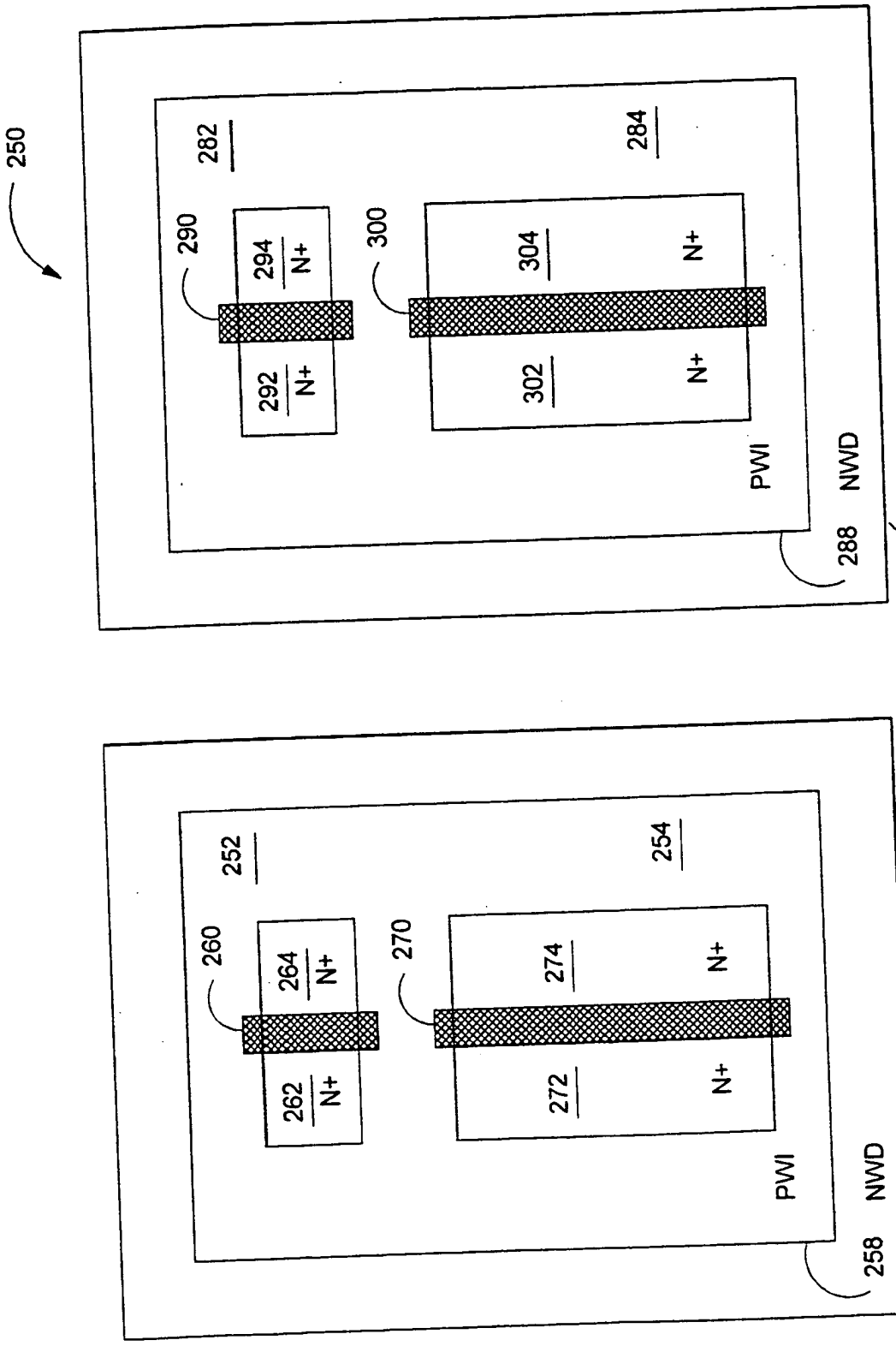

250
282
284
290
294
N+
292
N+
300
304
N+
302
N+
PWI
NWD
286
288
252
254
260
264
N+
262
N+
270
274
N+
272
N+
PWI
NWD
256
258

FIG.4

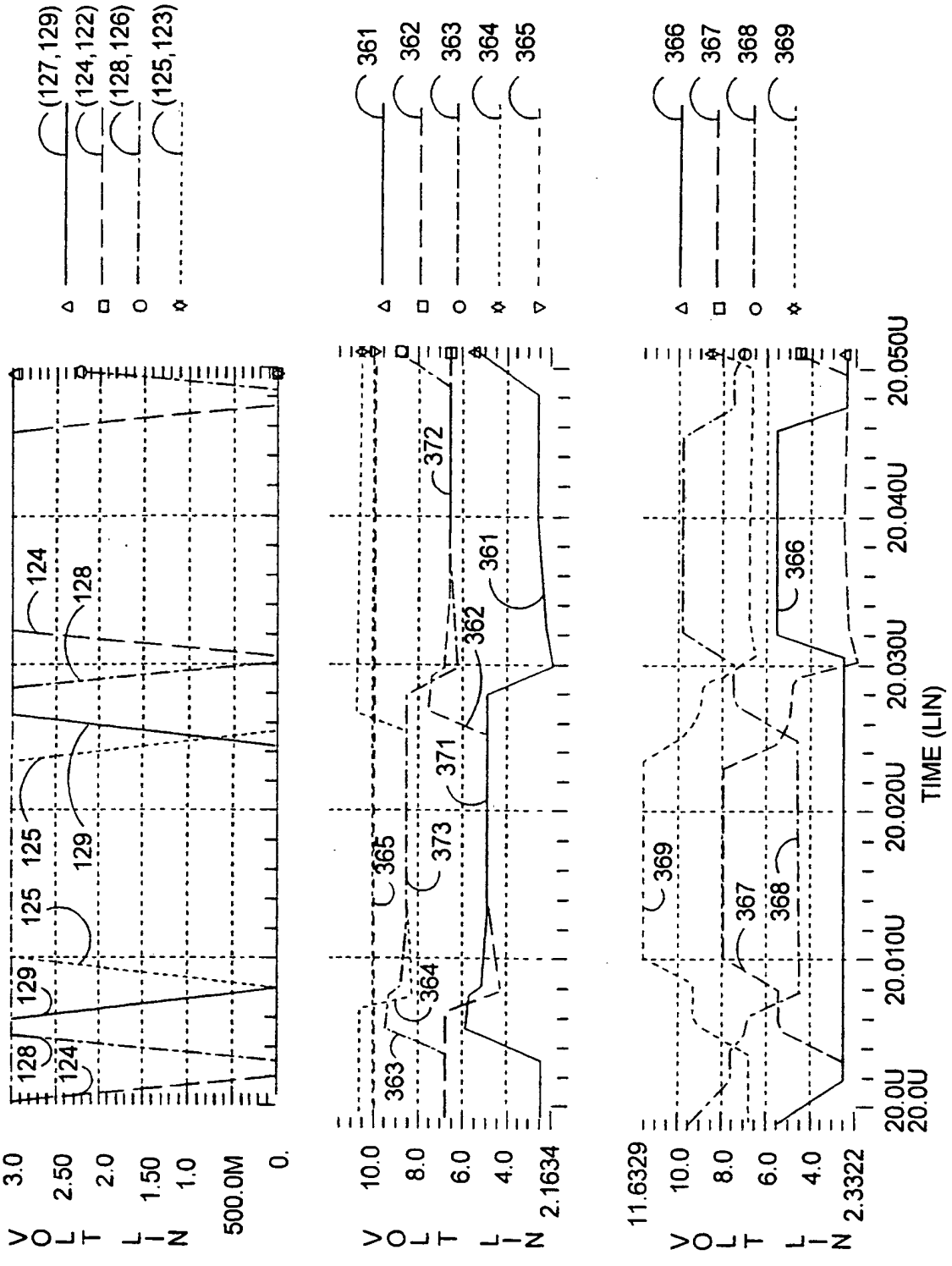
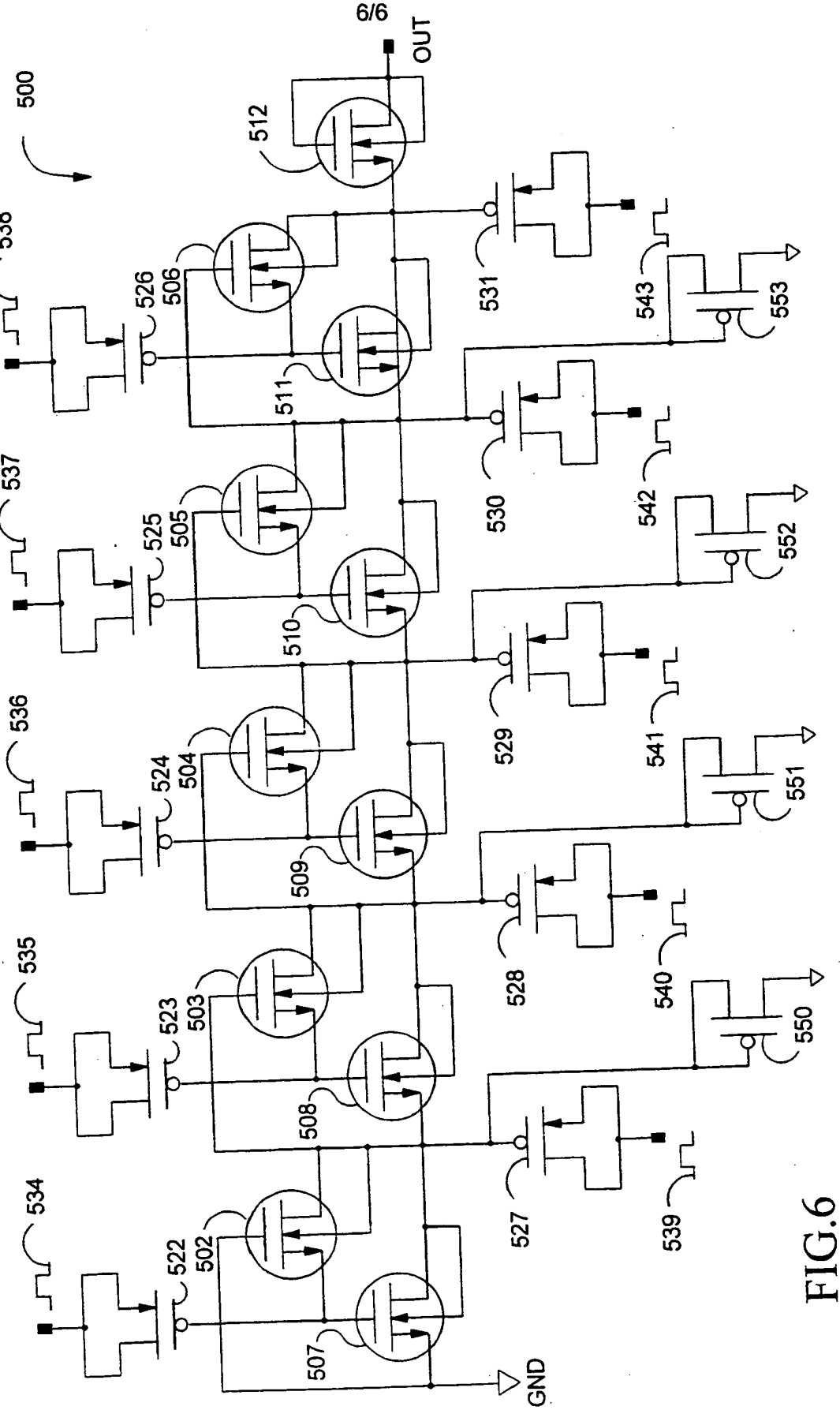


FIG.5A

FIG.5B

FIG.5C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GND

FIG.6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/16317

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO3K 17/56, 17/687, 17/74; HO1L 29/788
US CL : 257/316, 321; 327/530, 536, 537
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/316, 321; 327/530, 536, 537

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 5,489,870 A (Arakawa) 02 February 1996, col.1, lines 17-20 and col.7, lines 32-36.	1-8 --- 9-13
Y	US 5,502,629 A (Ito et al) 26 March 1996, see entire document.	9-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 FEBRUARY 1997	21 FEB 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WAEL FAHMY Telephone No. (703) 308-4918